1. A radio frequency (RF) multi-antenna access point enhancement circuit comprising:

a multi-antenna signal processing circuit situated in a first access point and adapted to:

(a) operate simultaneously with a first baseband processor, so that said first baseband processor handles data transmissions in a first mode between said first access point and a second access point under a first channel transmission condition, and said multi-antenna signal processor handles data transmissions in a second mode between said first access point and said second access point under a second channel transmission condition;

(b) receive M independent RF modulated input signals from said second access point when the second channel transmission mode exists between the first access point and said second access point;

(c) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said multi-antenna signal processing circuit operates selectively with a first baseband processor to demodulate RF signals received in a channel from a second access point.

2. The circuit of claim 1, wherein said multi-antenna signal processing circuit is enabled and selectively operates in said second mode when channel conditions indicate that a data rate in said channel has fallen below a predetermined threshold.

3. The circuit of claim 1, wherein said multi-antenna signal processing circuit is enabled and selectively operates in said second mode in response to a determination that a data rate in said channel is to be enhanced above a nominal operating rate.

4. The circuit of claim 1, wherein said multi-antenna signal processing circuit is enabled and selectively operates in said second mode in response to a determination that frequency selective fading is present in said channel.

5. The circuit of claim 1 wherein said multi-antenna signal processing circuit is situated in a signal path ahead of said first baseband processor, and is further adapted to monitor channel transmission conditions.

6. The circuit of claim 1, wherein said first baseband processor is compatible with an 802.11x communications protocol.

7. The circuit of claim 1 wherein a processing latency of said multi-antenna signal processing circuit is compensated using a dummy data response to maintain compatability with a transmission protocol used by said first access point and said second access point.

8. The circuit of claim 1 wherein said multi-antenna signal processing circuit is configured as a multiple-in, multiple out (MIMO) processor.

9. The circuit of claim 1, wherein said multi-antenna signal processing circuit demodulates a data stream transmitted using multiple independent antennas which each transmit a portion of said data stream.

10. An 802.11x compatible radio frequency (RF) multi-antenna access point enhancement circuit comprising:

a multi-antenna signal processing circuit situated in a first access point and adapted to:

(a) operate simultaneously with a first baseband processor, so that said first baseband processor handles data transmissions in a first mode between said first access point in accordance with an 802.11x protocol, and a second access point under a first channel transmission condition, and said multi-antenna signal processor handles data transmissions in a second mode between said first access point and said second access point in accordance with an 802.11x protocol under a second channel transmission condition;

(b) receive M independent RF modulated input signals from said second access point when the second channel transmission mode exists between the first access point and said second access point;

(c) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

(d) transmit an RF modulated signal to said second access point using a point coordination function (PCF) mode associated with said 802.11x protocol so as to maintain timing compatibility;

wherein said multi-antenna signal processing circuit operates with a first baseband processor to receive and transmit RF signals in a channel between said first access point and said second access point.

11. The circuit of claim 10 wherein said multi-antenna signal processing circuit processes data using a high rate direct sequence spread spectrum (HR/DSSS) physical layer frame structure that has a preamble and header compatible with said 802.11x protocol.

12. The circuit of claim 11, wherein said header includes additional data to identify a high rate mode.

13. The circuit of claim 11, wherein said header includes additional data to identify a modulation format.

14. The circuit of claim 10, wherein said first baseband processor sends multicast transmissions to a first set of targets within a first range of said first access point, and said multi-antenna signal processing circuit sends multicast transmissions to a second set of targets within a second range of said first access point.

15. The circuit of claim 10, wherein first baseband processor communicates with a first set of targets during a first access period, and said multi-antenna signal processing circuit communicates with a second set of targets during a second access period.

16. The circuit of claim 15, wherein said first access period and said second access period are alternated at a predetermined ratio.

17. The circuit of claim 10, wherein said multi-antenna signal processing circuit uses a wave beam transmission to communicate selectively to a target in a specific location, and not to other targets.

18. The circuit of claim 10, wherein said multi-antenna signal processing circuit is incorporated as part of a closed circuit television monitoring system, and said M independent signals are transmitted by N individual cameras.

19. The circuit of claim 10, wherein a receive sensitivity of said first access point can be improved by selectively adding additional multi-antenna signal processing circuit modules for a data transmission, and/or increasing M.

20. A radio frequency (RF) multi-antenna access point circuit comprising:

a baseband processor circuit for handling data transmissions during a first operating mode in a channel between a first access point and a second access point;

a multi-antenna signal processing circuit for handling data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to:

(a) receive M independent RF modulated input signals from said second access point;

(b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said first operating mode and said second operating mode are automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel;

a modulator/demodulator circuit coupled to an antenna assembly and said multi-antenna signal processing circuit and baseband processor circuit for extracting I/Q data samples from an RF modulated received signal;

a media access controller coupled to said multi-antenna signal processing circuit and baseband processor circuit for interfacing to a host computing system.